a third semiconductor layer formed on said second insulation layer and composing said control gate,

the third semiconductor layer, the second insulation layer, and the second semiconductor layer being etched using a single photoresist film as a mask.

5. (Once Amended) The non-volatile semiconductor storage apparatus according to claim 1, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells.

6. (Once Amended) The non-volatile semiconductor storage apparatus according to claim 2, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells.

REMARKS

Claims 1, 3, and 5-7 were rejected under 35 U.S.C. §112, second paragraph. Claims 1, 5, and 6 were rewritten to overcome this rejection.

Claims 1-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,604,367 to Yang, in view of U.S. Patent No. 6,091,634 to Wong. Claim 1 provides that the top and bottom surfaces of the floating gate and the control gate in the position where the floating gate and the control gate extend above the gate of the select field effect transistor are parallel to the top and bottom surfaces of the gate of the select field effect transistor. In contrast, in Yang, floating gate 42 and the control gate 70 in the position above the gate 24' of the select field effect transistor do not have top and bottom surfaces parallel to the top and bottom surfaces

of the gate of the select field effect transistor, (see Yang, Figs. 8B and 11, and Office Action, page 4, lines 1-11).

Claim 2 provides that the first insulation layer which insulates the first semiconductor layer from the second semiconductor layer in the select field effect transistor contacts the first semiconductor layer. In contrast, in Yang, the first insulation layer, according to the Examiner 28', does not contact the first semiconductor layer 24, (see Yang, Fig. 11, and Office Action, page 4, lines 3-8).

In addition, claims 1 and 2 provide that an insulating layer below the floating gate of the memory cell is used as a tunneling gate oxide layer in contrast to Yang, which only discloses a tunneling layer being formed between T1 and T2.

In the present invention, as shown in Figs. 7G and 7H, and as claimed in claim 2, the second semiconductor layer 13 is formed on the first semiconductor layer 6, and the second semiconductor layer 13 is formed so that its lower surface is always located on or above the upper surface of the first semiconductor layer 6 (and, parallel to the first semiconductor layer 6 surface). In other words, the second semiconductor layer 13 of a part of the floating gate is formed so as to be always located higher than the height of the first semiconductor layer 6 of the memory cell transistor and select transistor.

Although the second semiconductor layer 42 is partially formed on the first semiconductor layer 24 in Fig. 8B of Yang, since the second semiconductor layer 42 must be connected to the tunnel oxide film 39' at a region between T1 and T2, the lower surface of second semiconductor layer 42 is located lower than the upper surface of first semiconductor layer 24 at a location where the tunnel oxide film 39' and second semiconductor layer 42 are connected to each other. Moreover, although in both Yang and the present invention, the first

semiconductor layer and the second semiconductor layer form a floating gate, the second semiconductor layer 42 is connected to the tunnel film in Yang, whereas the second semiconductor layer 13 does not contact the tunnel film in the present invention. Instead, the first semiconductor layer 6 is connected to the tunnel film in the present invention.

Claim 2 also provides that the third semiconductor layer, the second insulation layer, and the second semiconductor layer are etched using a single photoresist film as a mask, which is supported, for example, in the specification on page 19, lines 5-11.

Referring to the previously mentioned portion of the specification, the photoresist 17 is patterned so as to cover the select field effect transistor Tr as a mask, and the polysilicon film 16 (the third semiconductor layer composing the control gate), ONO film 15 (the second insulation layer), and polysilicon film 13 (the second semiconductor layer composing a portion of the floating gate), are etched. In other words, the claimed feature is that the control gate, a portion of the floating gate, and the ONO film which insulate those gates are formed in single resist patterning by, for example, resist 17.

The Yang invention cannot form both the control gate and floating gate in single resist patterning. With the resist mask 44" as a mask, the polysilicon 44 is etched to form the floating gate as shown in Fig. 7B, and with the resist mask 52" as a mask, the polysilicon 52 is etched to form the control gate as shown in Fig. 8B. It is apparent that the control gate and floating gate cannot be formed unless mask patterning is carried out twice, and an error will be inevitably produced in mask alignment.

The single resist patterning feature claimed in claim 2 is crucial, and this results in process simplification and a reduction in production tolerance, and consequent stabilization of characteristics. The degree of overlapping between the second semiconductor layer and the third

semiconductor layer greatly influences the characteristics, and this production tolerance can be reduced by employing a single resist process.

CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claims 1 and 2 are in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,

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Enclosure: Version With Markings to Show Changes Made
Amended Figs. 4 and 5

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraphs beginning on page 19, line 17, and ending on page 20, line 27, have been rewritten as follows:

Then, a silicon oxide film is [filly] fully stacked, and the stacked film is etched back, whereby a side wall (not shown) is formed laterally of the gate electrode in the peripheral circuit region. At the same time, as shown in Fig. 7I, a side wall 18 composing of an oxide film is formed laterally of the polysilicon film 16, ONO film 15, and polysilicon film 13. Further, in the peripheral circuit region, the side wall is defined as a mask, and ion-implantation with high density is carried out, thereby forming a transistor with an LDD structure. Further, an interlayer insulation film 19 consisting of a BPSG (boron-doped phosphor-silicate glass) film, for example, is stacked by a CVD method. The thickness of the interlayer insulation film 19 is about 8000 to 10000 Angstroms, for example. Next, as shown in Fig. 8E, contact holes 20 reaching the N^+ diffusions 9b are formed in the interlayer insulation film 19 and silicon oxide film 11, wiring layers 21 are embedded in the [control] contact holes 20, and a wiring layer 22 commonly connecting the wiring layers is further formed as a bit line BL. The wiring layers 21 and 22 are made of an aluminum alloy, for example, and the thickness of the wiring layer 22 is about 4000 to 6000 Angstroms, for example. As a source, a source line is formed commonly by the N^+ diffusion layer 9a. In addition, the N^+ diffusion layer 9b and wiring layer 21 are shared between the adjacent memory cell transistors in the columnar direction (transverse direction in Fig. 7I).

In addition, contact holes (not shown) [is] are opened reaching the N^+ diffusion layer 9a that is a source by several bits at the same time when the contact hole 20 is formed, and the contact holes are embedded by the wiring layer 21. A stay of the wiring layer 22 is provided,

and further, an interlayer insulation film is fully formed. Then, a contact hole 23 is formed so as to reach the stay of the wiring layer 22 formed in a source region prior to this interlayer insulation film, is embedded by a wiring layer (not shown), and is commonly connected in a wiring layer, thereby making it possible to make a resistance of a common source line lower than that in a case of only an N^+ diffusion layer.

IN THE CLAIMS

Please rewrite claims 1, 2, 5, and 6, as follows:

1. (Once Amended) A non-volatile semiconductor storage apparatus comprising:

a memory cell array which has unit cells arranged in a rectangular matrix shape, said unit cell including:

a memory cell field effect transistor having a floating gate and a control [gate;] gate, an insulating layer below said floating gate being used as a tunneling gate oxide layer; and

a select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said floating gate and control gate extending to a position above a gate of said select field effect [transistor.] transistor, top and bottom surfaces of said floating gate and said control gate in said position being parallel to top and bottom surfaces of said gate of said select field effect transistor.

2. (Once Amended) A non-volatile semiconductor storage apparatus having a memory cell array having unit cells, said unit cell including a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate and a control gate, an insulating layer below said floating gate being used as a tunneling gate oxide layer, and

said select field effect transistor having a drain connected to a source of said memory cell field effect transistor, said storage apparatus comprising:

a first semiconductor layer composing a portion of said floating gate and a gate of said select field effect transistor;

a second semiconductor layer formed on said first semiconductor layer in said memory cell field effect transistor, said second semiconductor layer not contacting said tunneling gate oxide layer, a lower surface of said second semiconductor layer being located at a height at least equal to a height of an upper surface of said first semiconductor layer, said second semiconductor layer composing another portion of said floating gate and extending to a position above said gate of said select field effect transistor;

a first insulation layer which insulates said first semiconductor layer from said second semiconductor layer in said select field effect [transistor;] transistor, said first insulation layer contacting said first semiconductor layer; object to this

a second insulation layer formed on said second semiconductor layer; and

a third semiconductor layer formed on said second insulation layer and composing said control [gate.] gate,

the third semiconductor layer, the second insulation layer, and the second semiconductor layer being etched using a single photoresist film as a mask.

5. (Once Amended) The non-volatile semiconductor storage apparatus according to claim 1, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a [second] first direction in said unit cells.

6. (Once Amended) The non-volatile semiconductor storage apparatus according to claim 2, further comprising a drain diffusion layer shared between adjacent memory cell field effect transistors in a [second] first direction in said unit cells.